DETAILED DESCRIPTION

[Detailed description]
[0001]
[Field of the Invention] this invention relates to the manufacture technique of light emitting devices, such as Light Emitting Diode and LD, of having the manufacture technique of a semiconductor substrate that a detailed quality semiconductor substrate is efficient and is obtained and high brightness, and high-reliability, about the manufacture technique of a semiconductor substrate, and the manufacture technique of a light emitting device.
[0002]
[The conventional technique] Among the semiconductors used for photogenesis devices, such as Light Emitting Diode and LD, etc., nitride system semiconductors, such as AlN, GaN, and InN, can be used, for example as such mixed crystal, and according to this, it has the advantage that it is possible to correspond to the photogenesis field of until [red to] ultraviolet. When manufacturing the semiconductor substrate for light emitting devices as this nitride system semiconductor, using typical GaN, the technique which is shown in drawing 4 is used conventionally. This technique forms the buffer layer 2 which consists of ZnO etc. on the substrate 1 which consists of sapphire etc. as shown in drawing 4 (a). Subsequently, as shown in drawing 4 (b), it is HVPE (Hydride Vapor Phase Epitaxy) about the GaN layer 4 on this buffer layer 2. After carrying out high-speed growth by the method etc., As shown in drawing 4 (c), the etching elimination of the above-mentioned buffer layer 2 is carried out with an acid etc., and GaN substrate S is obtained.
[0003] According to the above-mentioned technique, it is able to **** quality GaN with 1.4%, by the a-axis, since the rate of grid mismatching of GaN/ZnO is good.
[0004]
[Object of the Invention] However, although it is satisfactory in the above-mentioned technique if it is the case where small GaN is ****ed, as shown in Table 1 Since a crack occurs in GaN in the process which cools this after a difference's being in the lattice constant and coefficient of thermal expansion of GaN and ZnO, and silicon on sapphire and growing up large-sized GaN at the temperature [sake / this /, for example, it is about 1090 degrees C, / temperature], There is a problem that large-sized GaN substrate is not obtained by the above-mentioned technique.
[0005]
[Table 1]

	格子定数		熱膨張係数	
	a軸	c軸	c軸	c軸直交
GaN	3.186A	5.185A	7.8E(-6)	5.6E(-6)
ZnO	3.250A	5.2065A	———	———
サファイア	4.758A	5.182A	8.5E(-6)	7.5E(-6)

[0006] The purpose of this invention is to offer the manufacture technique of the manufacture technique of a semiconductor substrate which can manufacture a quality semiconductor substrate and the high brightness which used this semiconductor substrate, and the light emitting device which has high-reliability, without canceling the above-mentioned technical probrem and generating a crack etc.
[0007]
[The means for solving a technical problem] The above-mentioned purpose is attained by the manufacture technique of the semiconductor substrate of this invention shown below, and the manufacture technique of a light emitting device. That is, the

manufacture technique of the semiconductor substrate of this invention forms a buffer layer on the substrate for semiconductor stratification, and subsequently to a it top, after forming two or more outcrops by forming a mask partially with the material with which a crystal cannot grow up to be this buffer layer front face substantially, it has the process which forms a semiconductor layer in this outcrop. Moreover, the manufacture technique of the light emitting device of this invention has the process which forms the multilayer section which has a semiconductor barrier layer and a semiconductor clad layer on the semiconductor substrate obtained by the above-mentioned technique.

[0008]

[Operation] By dividing a semiconductor layer into a plurality and forming on a substrate, this invention makes small oval influence by the difference between the lattice constant of this semiconductor layer and the substrate for semiconductor stratification, or a coefficient of thermal expansion, and, thereby, prevents occurrence of a crack etc.

[0009] Drawing 1 is the schematic diagram showing an example of the manufacture technique of the semiconductor substrate of this invention. Hereafter, based on this drawing, this invention is explained in detail. In addition, the same sign is attached and explained to the same part as aforementioned drawing 4 in the following explanations.

[0010] (1) **** of a buffer layer -- first, as shown in drawing 1 (a), form the buffer layer 2 on the substrate for semiconductor stratification 1

[0011] When what has the as near crystal and as near lattice constant which constitute the semiconductor layer 4 and the buffer layer 2 which mean formation as the above-mentioned substrate for semiconductor stratification 1 as possible obtains the good semiconductor layer 4, it is desirable, and it is desirable to use what has still as near a coefficient of thermal expansion as possible when preventing occurrence of a crack etc. As the above-mentioned substrate for semiconductor stratification 1, it is a periodic table, for example. The compound (the following and an III-V group crystal are called) which the element of III group (only henceforth III group) and V group (only henceforth V group) combined at a rate of 1:1, sapphire, a crystal, SiC, etc. are mentioned. In addition, about 10-1000 micrometers, especially although it is not limited, when especially thickness of the substrate for semiconductor stratification 1 is set to about 20-700 micrometers, it becomes [fully] cheap economically and is desirable [thickness / the mechanical strength of this substrate 1]. moreover -- although especially the surface area by the side of semiconductor layer 4 formation of the substrate for semiconductor stratification 1 is not limited, either -- 0.3x0.3cm2 -20x20cm2 a grade -- more -- desirable -- 0.5x0.5cm2 -10x10cm2 The stable yield is also obtained, while a good semiconductor layer can be obtained, if it is a grade.

[0012] The above-mentioned buffer layer 2 is for easing the difference between the lattice constant between the substrate for semiconductor stratification 1, and the semiconductor layer 4, or a coefficient of thermal expansion. For this reason, when the thing with each crystal and lattice constant as near as this buffer layer 2 which constitute the substrate for semiconductor stratification 1 and the semiconductor layer 4 as possible obtains the good semiconductor layer 4, it is desirable, and it is desirable to use what has still as near a coefficient of thermal expansion as possible when preventing occurrence of a crack etc. As the above-mentioned buffer layer 2, a ZnO, MgO, BeO, and BeO-ZnO system compound, a ZnO-HgO system compound, a ZnO-MgO system compound, a BeO-ZnO-HgO system compound, a BeO-ZnO-MgO system compound, etc. are illustrated. Although formation of the above-mentioned buffer layer 2 is performed by technique, such as sputtering, and CVD, MOVPE, when using ZnO, a BeO-ZnO system compound, or a BeO-ZnO-HgO system compound, for example as a buffer layer 2 and this buffer layer 2 is formed by sputtering, it is desirable in respect of the elimination nature by etching of this buffer layer 2, and when it forms by MOVPE on the other hand, the crystallinity of this buffer layer 2 can be made good, and it is desirable. As for the above-mentioned buffer layer 2, it is desirable to form preferably, 10-2000nm in thickness, so that it may be set to 20-1500nm. If the thickness of the above-mentioned buffer layer 2 is 10nm or more, the difference between the lattice constant of the substrate for semiconductor stratification 1 and the semiconductor layer 4 or a coefficient of thermal expansion can fully be eased, and if it is 2000nm or less on the other hand, it is easy to remove this buffer layer 2 after semiconductor layer 4 formation.

[0013] (2) formation of a mask -- as shown in the occasion and drawing 1 (b), form a mask 3 in the buffer layer 2 above-mentioned front face partially, and form two or more outcrops 21

[0014] The above-mentioned mask 3 is not made not to grow up a crystal, in this invention, is forming this mask 3 partially on buffer layer 2 front face, and is made to expose buffer layer 2 front face on it in two or more places. Thus, if a crystal is grown up on the buffer layer 2 which formed the mask 3 partially, a crystal will grow up to be only the fraction (outcrop 21) which this plurality exposed. Therefore, it is enabled to divide and form the semiconductor layer 4 in a plurality by this.

[0015] The material which constitutes the above-mentioned mask 3 needs on it to be that a crystal cannot grow up to be substantially. As such a material, the amorphous field is illustrated and they are SiO2, Si3 N4, TiN, and Ta2 O5 as this amorphous field further. SiO2 with it being cheap especially and easy although a nitride, an oxide film, etc. of a grade are illustrated excelling in thermal resistance upwards and forming as a mask It is used especially suitably. The above-mentioned mask 3 can be formed by removing only the fraction which means formation of an outcrop 21 by technique, such as lithography, after forming so that the whole buffer layer 2 front face may be worn by technique, such as a spatter and CVD. Moreover, it is appropriate for the thickness of this mask 3 to be referred to as about 0.5-5 micrometers so that it may fully become easy the to form the function as a mask. Furthermore, although especially the flat-surface configuration of a mask 3 is not limited, if it is made into the shape of a grid which is shown in drawing 2 , since it can use buffer layer 2 surface area effectively, it is efficient, can manufacture the semiconductor layer 4, i.e., a semiconductor substrate, and becomes good [the yield].

[0016] It is desirable below 20mm angle grade and that each size of the above-mentioned outcrop 21 serves as below 5mm angle grade preferably. If each size (namely, each size of the semiconductor layer 4 by which split formation is carried out) of the

above-mentioned outcrop 21 is below 20mm angle, for a parvus reason, the oval influence by the difference between the lattice constant of the semiconductor layer 4 and the substrate for semiconductor stratification 1 or a coefficient of thermal expansion can prevent occurrence of the crack in the semiconductor layer 4 etc. Furthermore, the yield can be raised while the simplification of a manufacturing process and a reduction of a manufacturing cost will be attained since the process which carries out the dicing of the semiconductor layer 4 to a chip size becomes unnecessary if each size of the above-mentioned outcrop 21 is made into chip sizes (300-500 micrometer angle), such as a light emitting device. Moreover, the spacing of the above-mentioned outcrop 21 has desirable about 1-500 micrometers, if this spacing is above-mentioned within the limits, does not have the overgrowth of the semiconductor layer 4 on a mask 3, either, and can also hold down a manufacturing cost low.

[0017] (3) As shown in drawing 1 (c) after this [of a semiconductor layer / formation], form the semiconductor layer 4 in this outcrop 21.

[0018] There is especially no limit in the modality of semiconductor which can be formed as the above-mentioned semiconductor layer 4, for example, it is typical as a compound semiconductor. Although what consists of a compound (for example, GaN, GaP, GaAsP, AlGaAs) of an III-V group system etc. is illustrated The technique of this invention is useful especially although the semiconductor which consists of BN, AlN, GaN, or InN without what has a lattice constant near as a substrate for forming the semiconductor which consists of this compound also in the above-mentioned compound is formed.

[0019] In addition, in this invention, although there is especially no limit in the material used as the above-mentioned semiconductor layer 4, the aforementioned buffer layer 2, and the aforementioned substrate for semiconductor stratification 1, it is desirable to use mutually what has as near a lattice constant as possible from the ground mentioned above combining what has still as near a coefficient of thermal expansion as possible. What such a lattice constant and a coefficient of thermal expansion show, for example in Table 2 as combination of a near material mutually is mentioned.

[0020]

[Table 2]

半導体層	バッファ層	半導体層形成用基板
BN	BeO	サファイア
AlN	BeO-ZnO	サファイア
GaN	BeO-ZnO	サファイア
InN	ZnO-HgO	サファイア
InGaN	BeO-ZnO-HgO	サファイア
InAlN	BeO-ZnO-HgO	サファイア
InBN	BeO-ZnO-HgO	サファイア
GaAlN	BeO-ZnO	サファイア
GaBN	BeO-ZnO	サファイア
AlBN	BeO-ZnO	サファイア
InGaAlN	BeO-ZnO-HgO	サファイア
InGaBN	BeO-ZnO-HgO	サファイア
InAlBN	BeO-ZnO-HgO	サファイア
GaAlBN	BeO-ZnO	サファイア
InGaAlBN	BeO-ZnO-HgO	サファイア

[0021] Although HVPE, MOVPE, MBE, etc. are illustrated as the formation technique of the above-mentioned semiconductor layer 4, when forming what HVPE or MOVPE is suitably used when forming GaN, InN, or InGaN as a semiconductor layer 4, and added aluminum or B to AlN, BN, or the above GaN, InN, or InGaN, MOVPE is used suitably.

[0022] The above (1) The above-mentioned buffer layer 2 is removed after the process of - (3), the semiconductor layer 4 is taken out, and this is set to semiconductor substrate S (not shown). Although what is necessary is just to perform elimination of the buffer layer 2 by technique, such as etching by the acid, alkali, etc., a disconnection well-known in addition to this, and cutting, in order to make the semiconductor layer 4 separate from the substrate for semiconductor stratification 1 completely, being based on etching is desirable.

[0023] In this invention, light emitting devices, such as Light Emitting Diode and LD, can be manufactured by forming the multilayer section which has a semiconductor barrier layer and a semiconductor clad layer on semiconductor substrate S obtained by the above-mentioned technique.

[0024] Drawing 3 is the type-section view showing an example of the manufacture technique of the light emitting diode (Light Emitting Diode) by the above-mentioned technique. Hereafter, based on this drawing, the manufacture technique of the light

emitting device of this invention is explained.
[0025] (Production of semiconductor substrate S) First, as it is shown in drawing 3 (a) - (c), semiconductor substrate S is produced. In this invention, the explanation is omitted here that production of this semiconductor substrate S should just apply the completely same process as the above mentioned thing.
[0026] (Formation of the multilayer section) Subsequently to drawing 3 (d), on semiconductor substrate S obtained at the above-mentioned process, the semiconductor clad layer 51, the semiconductor barrier layer 52, and the semiconductor clad layer 53 are ****ed in this order, and the multilayer section 5 which has pn junction section X is formed so that it may be shown.
[0027] Since the clad layer formed in the barrier-layer upper and lower sides will not absorb the photogenesis from this barrier layer and the electron and electron hole for photogenesis will be efficiently confined in a barrier layer as a configuration of the above-mentioned multilayer section 5 if it is DH type especially although Homo type, SH (single hetero) type, DH (double hetero) type, the quantum well type, the multilayer quantum well type, etc. are possible, the brightness of a light emitting device can be raised.
[0028] As combination of the semiconductor material which constitutes above-mentioned barrier-layer 52 / clad layers 51 and 53, the above-mentioned semiconductor substrate S and what has a lattice constant near if possible are desirable, for example, when semiconductor substrate S consists of GaN, InGaN / InGaN [GaN and]/InGaAlN is suitable.
[0029] As the formation technique of the above-mentioned multilayer section 5, although MOVPE, MBE, GS-MBE, MO-MBE, CBE, HVPE, etc. are possible, when this multilayer section 5 consists of InGaN/GaN as mentioned above, for example, MOVPE is used suitably.
[0030] After forming the multilayer section 5 as mentioned above, as it is shown in drawing 3 (e), the buffer layer 2 is removed, the up electrode 6 is formed in multilayer section 5 top, the lower electrode 7 is formed in a semiconductor substrate S inferior surface of tongue, and light emitting diode D is obtained.
[0031] the case where the number of direct lower layers of the above-mentioned up electrode 6 is p -- AuBe, AuZn, Au, etc. -- moreover, when the number of direct lower layers is n, after -ed **ing AuGe, In, etc. with vacuum deposition etc. on the multilayer section 5 top, it is formed by fabricating in configurations arbitrary in the suitable position of this field by processing of patterning, an annealing, etc. Although especially the configuration of the section electrode 6 besides is not limited, it is desirable to consider as a dot-like electrode from the easy thing of formation etc.
[0032] Moreover, when there are p right above layers and there are n right above layers again about AuBe, AuZn, Au, etc., the above-mentioned lower electrode 7 is formed by making it alloy with semiconductor substrate S by annealing processing, after -ed **ing AuGe, In, etc. on the semiconductor substrate S inferior surface of tongue.
[0033] Although the dicing of the layered product in which the above-mentioned electrode was formed is carried out, it is chip-ized and being considered as light emitting diode, if it forms in production of the aforementioned semiconductor substrate S so that it may become a chip size beforehand about an outcrop 21, the process which carries out dicing will become unnecessary. Moreover, although the above-mentioned multilayer section 5 can also be formed after removing the buffer layer 2 when forming an outcrop 21 in a certain amount of size (for example, 3-20mm angle grade), according to this, there is a dislike which is a little inferior to manufacture luminous efficacy.
[0034] In addition, in this invention, light emitting devices, such as laser diode (LD), can also be manufactured besides light emitting diode as well as the above.
[0035] As mentioned above, in the manufacture technique of the light emitting device of this invention, the oval influence by the difference of the lattice constant with the substrate for semiconductor stratification or a coefficient of thermal expansion is small by dividing and forming a semiconductor layer in a plurality. Therefore, it is hard coming to generate a crack etc. in a semiconductor layer.
[0036]
[Example] Hereafter, an example is shown and this invention is explained more concretely. In addition, these examples do not limit this invention at all.
On silicon on sapphire with an example 1 thickness of 300 micrometers, ZnO layer with a thickness of 100nm was formed by sputtering. Subsequently, it is this ZnO layer SiO2 It covers and is SiO2 by lithography. A large number were removed in the part and ZnO layer was exposed (the amount of this outcrop could be 10mmx10mm, respectively). Subsequently, GaN layer with a thickness of 200 micrometers was formed by HVPE under the temperature of 1090 degrees C on exposed ZnO layer. Then, the etching elimination of the ZnO layer was carried out with the aqua regia, and GaN substrate was obtained.
[0037] It sets in the example of comparison 1 above-mentioned example 1, and is ZnO layer SiO2 It did not cover but GaN substrate was similarly obtained except [all] forming a direct n type GaN layer the whole surface on this ZnO layer.
[0038] In the example 2 - the 5 above-mentioned example 1, the semiconductor substrate was similarly manufactured except [all] changing to what shows silicon on sapphire, ZnO layer, and GaN layer in Table 3, respectively.
[0039]
[Table 3]

		構成材料			クラック等の発生の程度*
		半導体層	バッファ層	基板	
実施例	1	GaN	ZnO	サファイア	A
	2	GaN	BeO-ZnO	サファイア	A
	3	InN	ZnO	サファイア	A
	4	InN	ZnO-HgO	サファイア	A
	5	InGaN	BeO-ZnO-HgO	サファイア	B
	6	InGaN/GaN	ZnO	サファイア	B
比較例	1	GaN	ZnO	サファイア	C

*クラック等の発生の程度は、以下の基準によった。
A：発生なし　B：僅かに発生あり　C：発生あり

[0040] On silicon on sapphire with an example 6 thickness of 300 micrometers, ZnO layer with a thickness of 100nm was formed by sputtering. Subsequently, it is this ZnO layer SiO2 It covers and is SiO2 by lithography. A large number were removed in the part and ZnO layer was exposed (the amount of this outcrop considered as the 300micrometerx300micrometer chip size, respectively). Subsequently, the n type GaN substrate with a thickness of 200 micrometers was formed by HVPE under the temperature of 1090 degrees C on exposed ZnO layer. Furthermore, the n type GaN clad layer with a thickness of 2 micrometers, the p type InGaN barrier layer with a thickness of 0.5 micrometers, and the p type GaN clad layer with a thickness of 0.5 micrometers were formed by MOVPE on this n type GaN substrate at this order, respectively. Then, the etching elimination of the ZnO layer was carried out with the aqua regia, and Light Emitting Diode chip was obtained.
[0041] About each of Light Emitting Diode chip obtained in the semiconductor substrate and the example 6 which were acquired in the above-mentioned examples 1-5 and the example 1 of a comparison, when existence, such as occurrence of a crack, was investigated after the cooling process after a crystal growth, the result shown in Table 3 was obtained.
[0042]
[Effect of the invention] According to the manufacture technique of the semiconductor substrate of this invention, since a semiconductor layer is divided and formed in a plurality, the oval influence by the difference of the lattice constant with the substrate for semiconductor stratification or a coefficient of thermal expansion is small, and it is hard to generate a crack etc. in a semiconductor layer. Therefore, while a high quality and a highly reliable semiconductor substrate are obtained, the yield also improves.
[0043] Moreover, the yield can be raised while the simplification of a manufacturing process and a reduction of a manufacturing cost are attained since the process which carries out the dicing of this after the semiconductor stratification at a chip size becomes unnecessary since each of the size can be beforehand made into a chip size in a desirable mode at the time of split formation of a semiconductor layer.
[0044] Furthermore, since according to the manufacture technique of the light emitting device of this invention a semiconductor substrate is produced by the same technique as the above and a light emitting device is produced using this semiconductor substrate, it is efficient and the light emitting device which has high brightness and high-reliability can be manufactured.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed description]
[0001]
[Field of the Invention] this invention relates to the manufacture technique of the gallium-nitride system compound semiconductor chip used for photogenesis devices, such as blue, green or red light emitting diode, and laser diode, and the gallium-nitride system compound semiconductor especially expressed with general formula InXAlYGa1-X-YN (0<=X<1, 0<=Y<1) on silicon on sapphire is related with the technique of cutting the gallium-nitride system compound semiconductor wafer by which the laminating was carried out in the shape of a chip.
[0002]
[Prior art] Generally the semiconductor chip which is a source of photogenesis is prepared on the stem at photogenesis devices, such as light emitting diode and a laser diode. As a material which constitutes a semiconductor chip, in the case of red, an orange, yellow, and green diode, GaAs, GaAlAs, GaP, etc. are known, and if it is blue diode, ZnSe, InAlGaN, SiC, etc. are known.
[0003] Conventionally, generally the dicer or the scriber is used for the equipment cut down for the chip for photogenesis devices from the wafer with which the laminating of the semiconductor material was carried out. After a dicer carries out direct full cutting of the wafer in rotation of the blade which is generally also called dicing saw and uses the edge of a blade as a diamond or cuts the slot of width larger than edge-of-a-blade width deeply (half cutting), it is equipment which breaks a wafer by external force. a both-way rectilinear motion of the needle which uses a nose of cam as a diamond as well as a scriber on the other hand -- a scribe line (scribe line) very thin to a wafer -- for example, after lengthening in a grid pattern, it is the equipment which breaks a wafer by external force
[0004] In case the above-mentioned semiconductor material is cut in the shape of a chip using these equipments, since there is cleavage nature in the "110" orientation, the crystal of zinc structure which does not carry GaP, GaAs, etc. can be easily separated in the shape of a chip by putting in a scribe line in this orientation with a scriber, using this property.
[0005] However, generally, since the laminating of the gallium-nitride system compound semiconductor was carried out on silicon on sapphire, it was difficult for the wafer not to have the property top cleavage nature of a sapphire crystal called hexagonal system, but to cut with a scriber. the so-called hetero-epitaxial structure which carried out the laminating of the gallium-nitride system compound semiconductor on sapphire as the gallium-nitride system compound semiconductor wafer was described above on the other hand, when cutting by the dicer -- it is -- lattice constant irregular ** -- it was large, and since coefficient of thermal expansion also differed, there was a problem that a gallium-nitride system compound semiconductor tends to separate from silicon on sapphire Furthermore, since Mohs hardness is about 9 and the very hard matter, a crack and a chipping become easy to generate both sapphire and a gallium-nitride system compound semiconductor in a cut surface, and it was not able to cut correctly.
[0006]
[Object of the Invention] If a wafer is correctly separable in the shape of a chip, since the output of a light emitting device and luminous efficacy can be raised and many chips will moreover be obtained from one wafer, without damaging the crystallinity of a gallium-nitride system compound semiconductor, a productivity can be raised. Therefore, this invention was made in view of such a situation, the place made into the purpose is faced separating the gallium-nitride system compound semiconductor wafer which uses sapphire as a substrate in the shape of a chip, the crack of a cut surface and occurrence of a chipping are prevented, a yield is good, and it is in offering the manufacture technique of a chip of obtaining a desired configuration and a size.
[0007]
[The means for solving a technical problem] The manufacture technique of the gallium-nitride system compound semiconductor chip of this invention The process which forms the first rate slot in a silicon-on-sapphire side in a desired chip configuration, The process which carries out the laminating of the gallium-nitride system compound semiconductor to the silicon-on-sapphire side in which the rate slot of the above first was formed, and creates a gallium-nitride system compound semiconductor wafer, In the position in which the rate slot of the above first was formed in the silicon-on-sapphire [of the aforementioned gallium-nitride system compound semiconductor wafer], or gallium-nitride system compound semiconductor layer side, and the agreeing position It is characterized by providing the process which newly forms the second rate slot, and the process which separates a gallium-nitride system compound semiconductor wafer in the shape of a chip along the rate slot of the above first, and the rate slot of the above second.
[0008] In the manufacture technique of this invention, in order to form the first rate slot and the second rate slot, technique, such

as half cutting by the scribe by the scriber and the dicer, can be applied, and laser etc. may be used. It is more desirable to usually adjust to 10% or less of a depth to the thickness of silicon on sapphire, although especially a rate depth of flute does not ask. When it is in the inclination that silicon on sapphire will become easy to break during gallium-nitride system compound semiconductor growth if the first rate slot is put in too much more deeply than the aforementioned rate and the second rate slot is similarly put in too much more deeply than the aforementioned rate, it is because it is in the inclination that it becomes difficult for a wafer to be cut in the shape of a chip, and to make the position of the second rate slot agree with the position of the first rate slot during rate slot formation.

[0009] Moreover, in order to form the first rate slot, it can also form using etching, such as wet etching and dry etching. In wet etching, if it is the mixed acid of a sulfuric acid and a phosphoric acid, and dry etching, for example, techniques, such as RIE (reactive ion etching), can be used. However, forming the mask of a predetermined configuration on silicon on sapphire so that it may become a desired chip configuration before performing etching cannot be overemphasized.

[0010] Next, the gallium-nitride system compound semiconductor wafer which carries out the laminating of the gallium-nitride system compound semiconductor using vapor growths, such as the MOCVD method and the MBE method, for example, has p-n junction on the silicon on sapphire in which the first rate slot was formed can be created. Although a crystalline good thing is obtained as a light emitting device by usually growing up on the silicon on sapphire by which the mirror polishing was carried out, a gallium-nitride system compound semiconductor If the first rate slot is beforehand formed in silicon on sapphire like this application, the crystallinity of the gallium-nitride system compound semiconductor of a fraction when it corresponds to the first rate slot position other mirror planes -- the gallium-nitride system compound semiconductor which carried out the laminating on uniform silicon on sapphire -- differing -- coming (it being in the inclination that crystallinity becomes bad, generally.) A wafer can be cut from the fraction from which this crystallinity is different.

[0011] Furthermore, it is desirable to grind after a gallium-nitride system compound semiconductor wafer creation and a silicon-on-sapphire side, and to make it thin. Furthermore, as for the thickness of the silicon on sapphire after polishing, adjusting to 150 micrometers or less is still preferably desirable 200 micrometers or less. Because, as described above, a gallium-nitride system compound semiconductor wafer has also with many the micrometers [some dozens of] thickness of the gallium-nitride system compound semiconductor by which the laminating of the thickness of silicon on sapphire was usually carried out 300-800 micrometers and on it, and the most is occupied by the thickness of silicon on sapphire. And as described above, since the laminating of the gallium-nitride system compound semiconductor is carried out on the material from which a lattice constant and coefficient of thermal expansion are different, it has the property which is very hard to cut. Therefore, if the thickness of silicon on sapphire is too thick, in case the second rate slot will be formed behind and a wafer will be separated, it is in the inclination it is hard coming to break by the position which made the first rate slot and the second rate slot agree. Then, a wafer can be made to dissociate in the chip configuration made into the agreement position of the aforementioned rate slot, i.e., the purpose, by grinding silicon on sapphire to aforementioned within the limits, and making it thin. Since the wafer itself will become easy to break during polishing if it is made not much thin although especially the lower limit of the thickness of a substrate does not ask, as a practical value, 50 micrometers or more are desirable.

[0012] As long as the second rate slot is a position corresponding to the first rate slot position, you may form it in any a gallium-nitride system compound semiconductor layer and silicon-on-sapphire side. If it forms in a gallium-nitride system compound semiconductor side, the fraction from which crystallinity is different is removable.

[0013]

[Operation] An operation of the manufacture technique of this invention is explained based on a drawing. So that drawing 1 or drawing 4 may be drawing which has and explains the process of the 1 manufacture technique of this invention in a type-section view and drawing 1 may become a predetermined chip configuration on the front face of silicon on sapphire 1 The status that the first rate slot 11 was formed is shown, and drawing 2 shows the status of the wafer which carried out the laminating of the gallium-nitride system compound semiconductor 2 on the silicon on sapphire in which the rate slot 11 was formed. Drawing 3 shows the status that ground the silicon-on-sapphire 1 side of the wafer of drawing 2 , and it was made thin, and drawing 4 shows the status that the second rate slot 22 was newly formed so that it might agree with the first rate slot 11 in the silicon-on-sapphire 1 side of the wafer of drawing 3 . In addition, in these drawings, the rate slots 11 and 22 are formed by the scribe.

[0014] [first, / the fraction of the first rate slot 11 / to divide, in case a wafer is behind separated since silicon on sapphire can be made thin by the depth of the first rate slot 11, while the chip configuration made into the purpose by forming the first rate slot 11 beforehand on the silicon on sapphire 1 before gallium-nitride system compound semiconductor growth is set up as shown in drawing 1] furthermore, the crystallinity of gallium-nitride system compound semiconductor 2' which grew up the exposed surface of the first rate slot 11 on the rate slot 11 since the mirror-plane nature of silicon on sapphire was lost and field azimuths also differed further -- a mirror plane -- it can be made to differ from the gallium-nitride system compound semiconductor 2 of most which was grown up on uniform silicon on sapphire

[0015] next, the gallium-nitride system compound semiconductor grown up on silicon on sapphire as shown in drawing 2 -- a mirror plane -- it consists of gallium-nitride system compound semiconductor 2' grown up on the gallium-nitride system compound semiconductor 2 grown up on uniform silicon on sapphire, and the first rate slot 11 Generally, the crystallinity of 2' section is worse than the crystallinity of the two sections, and it has the different property.

[0016] Next, sapphire can be made to divide by grinding silicon on sapphire 1 and making it thin, as shown in drawing 3 .

[0017] Next, the wafer is made to break by the position the first rate slot 11 and whose second rate slot 22 made silicon on sapphire thin by the depth of the second rate slot 22, and corresponded by newly forming the second rate slot 22 in a

silicon-on-sapphire 1 side in the position which agrees with the first rate slot 11 as shown in drawing 4 . [furthermore, / the gallium-nitride system compound semiconductor layer which hits 2' section as mentioned above / to divide a gallium-nitride system compound semiconductor from a bad crystalline fraction, since crystallinity is bad and differs from the gallium-nitride system compound semiconductor layer 2 of most with the sufficient crystallinity of others / property] [moreover, / a wafer / to be in the status that the rate slot entered doubly deeply, and to divide, since the gallium-nitride system compound semiconductor layer of bad crystalline 2' section can be removed when the second rate slot 22 is formed in the gallium-nitride system compound semiconductor layer 2 side]

[0018] That is, after the manufacture technique of this invention attaches a blemish to silicon on sapphire beforehand in the first rate slot and grows up a bad crystalline gallium-nitride system compound semiconductor into the blemish fraction, as a bad crystalline gallium-nitride system compound semiconductor layer is removed in the second rate slot or a wafer breaks toward a bad crystalline fraction, it is the technique of obtaining a chip, by preparing a new blemish (second rate slot) in a silicon-on-sapphire side, and cutting it.

[0019]

[Example] An adhesive tape is stuck on the silicon on sapphire of 400 micrometers in [example 1] thickness, and size [of 2 inches] phi, and it sticks on the table of a scriber, and fixes by the vacuum chuck. A table is movable in the X-axis (right and left) and the orientation of Y-axis (before or after), and has the structure which can be rotated. The scribe of the silicon on sapphire is carried out once to X shaft orientations in 500 micrometer pitch and the depth of 5 micrometers by the diamond stylus of a scriber after fixation. 90 degrees is rotated and the scribe of the table is shortly carried out like Y shaft orientations. Thus, a scribe line is put in so that it may become the chip of 500 micrometer angle, and the first rate slot is formed. However, sapphire makes the field which forms the first rate slot the field by which the mirror polishing was carried out.

[0020] Next, the aforementioned silicon on sapphire is set to an MOCVD system, and on silicon on sapphire, it grows up by the thickness of 5 in all micrometers, and let an n type GaN layer and a p type GaN layer be gallium-nitride system compound semiconductor wafers.

[0021] The silicon-on-sapphire side of a wafer is ground by the burnisher after growth, and a substrate is wrapped, and reaches and carries out a polishing in thickness of 150 micrometers. A substrate front face is made into mirror-plane homogeneity by the polishing, and it carries out as [check / the first rate slot / easily / from a silicon-on-sapphire side].

[0022] Next, an adhesive tape is stuck on GaN layer side, a scribe is similarly carried out once to the X-axis and Y-axis in 500 micrometer pitch and the depth of 5 micrometers with a scriber, and the second rate slot is formed. However, having carried out the scribe so that the position of the second rate slot may agree with the first rate slot cannot be overemphasized.

[0023] The vacuum chuck was released after the scribe, the wafer was removed from the table, and much chips of 500 micrometer angle were obtained from the wafer of 2 inch phi by pressing down with a roller lightly from a silicon-on-sapphire side. When a crack, a chipping, etc. did not occur in the cut surface of a chip but what has a poor appearance that is not was taken out, the yield was 95% or more.

[0024] In the process which forms the second rate slot of the [example 2] example 1, when the second rate slot was formed in the depth of 5 micrometers from GaN layer side, and also the chip of 500 micrometer angle was obtained similarly, similarly the yield was 95% or more.

[0025] In the process which grinds the silicon on sapphire of the gallium-nitride system compound semiconductor wafer of the [example 3] example 1, when silicon on sapphire was carried out in thickness of 200 micrometers, and also the chip of 500 micrometer angle was obtained similarly, the yield was 90% or more.

[0026] In the [example 4] example 1, when used the dicer and half cutting of both was carried out in the depth of 10 micrometers by dicing, when forming the first rate slot and the second rate slot, and also the chip of 500 micrometer angle was obtained similarly, the yield was 95% or more.

[0027] The mask 33 which consists of SiO2 is formed in the same silicon on sapphire of a size as the [example 5] example 1 by vacuum evaporationo in a configuration from which the chip of 500 micrometer angle is obtained using photo-lithography technique. The plan of the silicon on sapphire in which the mask 33 was formed is shown in drawing 5 . It is shown that this drawing forms the mask 33 of 500 micrometer angle on the squares in 50 micrometer pitch.

[0028] Next, it is immersed in the mixed acid of the sulfuric acid which heated the silicon on sapphire, and a phosphoric acid, the silicon on sapphire in which the mask 33 is not formed is etched in the depth of about 5 micrometers, and the first rate slot is formed. After etching, after are immersed in fluoric acid and removing a mask 33, a gallium-nitride system compound semiconductor wafer is created by the MOCVD method like an example 1.

[0029] When the silicon-on-sapphire side of a wafer was ground, the rate slot after [second] polishing was formed and the rest obtained the chip like the example 1, similarly the yield was 95% or more.

[0030]

[Effect of the invention] As explained above, according to the technique of this invention, by the technique of a scribe, a dicer, laser, etc., the gallium-nitride system compound semiconductor wafer which does not have cleavage nature can also be correctly cut with a sufficient yield, and its productivity improves.

[Translation done.]

DETAILED DESCRIPTION

[Detailed description]
[0001]
[Field of the Invention] The gallium-nitride system compound semiconductor which this invention requires for the manufacture technique of the gallium-nitride system compound semiconductor chip used for photogenesis devices, such as blue, green or red light emitting diode, and laser diode, especially is expressed with general formula InXAlYGa1-X-YN (0<=X<1, 0<=Y<1) on silicon on sapphire is related with the technique of cutting the gallium-nitride system compound semiconductor wafer by which the laminating was carried out in the shape of a chip.
[0002]
[Prior art] Generally the semiconductor chip which is a source of photogenesis is prepared on the stem at photogenesis devices, such as light emitting diode and a laser diode. As a material which constitutes a semiconductor chip, in the case of red, an orange, yellow, and green diode, GaAs, GaAlAs, GaP, etc. are known, and if it is blue diode, ZnSe, InAlGaN, SiC, etc. are known.
[0003] Conventionally, generally the dicer or the scriber is used for the equipment cut down for the chip for photogenesis devices from the wafer with which the laminating of the semiconductor material was carried out. After a dicer carries out direct full cutting of the wafer in rotation of the blade which is generally also called dicing saw and uses the edge of a blade as a diamond or cuts the slot of width larger than edge-of-a-blade width deeply (half cutting), it is equipment which breaks a wafer by external force. a both-way rectilinear motion of the needle which uses a nose of cam as a diamond as well as a scriber on the other hand -- a scribe line (scribe line) very thin to a wafer -- for example, after lengthening in a grid pattern, it is the equipment which breaks a wafer by external force
[0004] In case the above-mentioned semiconductor material is cut in the shape of a chip using these equipments, since there is cleavage nature in the "110" orientation, the crystal of zinc structure which does not carry GaP, GaAs, etc. can be easily separated in the shape of a chip by putting in a scribe line in this orientation with a scriber, using this property.
[0005] However, generally, since the laminating of the gallium-nitride system compound semiconductor was carried out on silicon on sapphire, it was difficult for the wafer not to have the property top cleavage nature of a sapphire crystal called hexagonal system, but to cut with a scriber. since a gallium-nitride system compound semiconductor wafer is the so-called hetero-epitaxial structure which carried out the laminating of the gallium-nitride system compound semiconductor on sapphire on the other hand as described above, when cutting by the dicer -- lattice constant irregular ** -- it was large, and since coefficient of thermal expansion also differed, there was a problem that a gallium-nitride system compound semiconductor tends to separate from silicon on sapphire Furthermore, since Mohs hardness is about 9 and the very hard matter, a crack and a chipping become easy to generate both sapphire and a gallium-nitride system compound semiconductor in a cut surface, and it was not able to cut correctly.
[0006]
[Object of the Invention] If a wafer is correctly separable in the shape of a chip, since the output of a light emitting device and luminous efficacy can be raised and many chips will moreover be obtained from one wafer, without damaging the crystallinity of a gallium-nitride system compound semiconductor, a productivity can be raised. Therefore, this invention was made in view of such a situation, the place made into the purpose is faced separating the gallium-nitride system compound semiconductor wafer which uses sapphire as a substrate in the shape of a chip, the crack of a cut surface and occurrence of a chipping are prevented, a yield is good, and it is in offering the manufacture technique of a chip of obtaining a desired configuration and a size.
[0007]
[The means for solving a technical problem] The manufacture technique of the gallium-nitride system compound semiconductor chip of this invention The process which forms at a line the protective coat which has the property in which a gallium-nitride system compound semiconductor does not grow up to be a front face in a desired chip configuration on silicon on sapphire, The process which is made to carry out the selective growth of the gallium-nitride system compound semiconductor, and creates a gallium-nitride system compound semiconductor wafer on the silicon on sapphire in which the aforementioned protective coat was formed, It is characterized by providing the process which cuts a gallium-nitride system compound semiconductor wafer from the fraction in which the aforementioned protective coat was formed, and is separated in the shape of a chip.
[0008] In the technique of this invention, it is desirable to also bear the growth temperature of a gallium-nitride system compound semiconductor, to use what thing for it, as long as it has the property in which a gallium-nitride system compound semiconductor does not grow into the material of the protective coat formed on silicon on sapphire, and to specifically use either a silicon dioxide

or silicon nitride. These materials can carry out pattern formation easily at a chip configuration using techniques, such as vacuum evaporationo and a spatter, by preparing a mask in a silicon-on-sapphire front face at a line.

[0009] Next, the gallium-nitride system compound semiconductor wafer which carries out the laminating of the gallium-nitride system compound semiconductor using vapor growths, such as the MOCVD method and the MBE method, for example, has p-n junction on the silicon on sapphire in which the protective coat was formed can be created. Although a gallium-nitride system compound semiconductor grows on sapphire, in order that it may not grow on a protective coat, the wafer which carried out the laminating of the gallium-nitride system compound semiconductor by which the selective growth was carried out so that it might become a desired chip configuration beforehand is obtained.

[0010] Next, it is separable from the fraction in which the aforementioned protective coat was formed in the shape of a chip by cutting a wafer. Especially cutting process cannot be asked, can apply technique, such as a scribe by the scriber, the half cutting by the dicer, and full cutting, and can also use laser etc. You may put in a cutting plane line from any a silicon-on-sapphire [of a wafer], and protective coat side. In addition, in case a cutting plane line is put in from a silicon-on-sapphire side, making the position of a cutting plane line in agreement with the position in which the protective coat was formed cannot be overemphasized. Moreover, before a disconnection, etching techniques, such as wet etching, may be used and the protective coat of a wafer may be removed. Since a scribe line can be directly put into the silicon-on-sapphire side where the protective coat exfoliated in case for example, a scribe line is put in from a protective coat side and a wafer is broken by removing a protective coat beforehand, it becomes [very] easy to divide and is desirable.

[0011] Furthermore, in case a cutting plane line is put in and cut from a gallium-nitride system compound semiconductor layer side, it is very desirable to form the line breadth of a protective coat beforehand more widely than the disconnection width of face of a gallium-nitride system compound semiconductor wafer in order not to damage a gallium-nitride system compound semiconductor. Especially in case this is cut from a protective coat side by the dicer, it is effective. Because, as compared with a scriber, the thickness of a dicer of a blade is some dozens times [several times to] large. Therefore, it is because a gallium-nitride system compound semiconductor will be damaged by the nose of cam of a blade to cut, the tooth side, etc. if the width of face of a protective coat is narrow, in case a wafer is cut from a protective coat side by the dicer with the large thickness of a blade. On the other hand, if the width of face of the fraction which exfoliated the protective coat is narrower than a scribe line even in case a scriber cuts, a gallium-nitride system compound semiconductor will be damaged at the nose of cam of a scriber. Moreover, when laser etc. cuts, it is more desirable than the diameter of a spot of laser similarly that the width of face of the fraction which exfoliated the protective coat is wide.

[0012] Moreover, it is desirable to grind a silicon-on-sapphire side after a gallium-nitride system compound semiconductor wafer creation and before a wafer disconnection, and to make it thin, and, as for the thickness of the silicon on sapphire after polishing, adjusting to 150 micrometers or less is still preferably desirable 200 micrometers or less. In case a scribe line is put in from a silicon-on-sapphire side using a scriber, and especially in case half cutting of this means is carried out from a silicon-on-sapphire side by the dicer, it is effective. It is because it is in the inclination that a wafer seldom breaks in case it will divide in the shape of a chip, if the thickness of silicon on sapphire is thicker than 200 micrometers. Moreover, if a wafer is ground and it is made thin in case full cutting is carried out by the dicer, laser, etc., compaction of disconnection time can be performed. Since the wafer itself will become easy to break during polishing if it is made not much thin although especially the lower limit of the thickness of a substrate does not ask, as a practical value, 50 micrometers or more are desirable.

[0013]

[Operation] An operation of the manufacture technique of this invention is explained based on a drawing. Drawing 1 or drawing 4 is drawing which has and explains the process of the 1 manufacture technique of this invention in a type-section view, the status that the protective coat 11 was formed in the line is shown, and drawing 2 shows the status of the wafer which was made to carry out the selective growth of the gallium-nitride system compound semiconductor 2, and carried out the laminating on the silicon on sapphire 1 in which the protective coat 11 was formed so that drawing 1 may become a predetermined chip configuration on the front face of silicon on sapphire 1. Moreover, drawing 3 shows the status that the protective coat 11 was exfoliated, and after drawing 4 grinds silicon on sapphire 1 and makes it thin while it exfoliates a protective coat 11, it shows the status that the scribe line was put into the silicon on sapphire 1 of the fraction into which the protective coat 11 exfoliated from the gallium-nitride system compound semiconductor layer 2 side.

[0014] As shown in drawing 1 and drawing 2 , the protective coat 11 a gallium-nitride system compound semiconductor does not grow up to be is formed on silicon on sapphire 1, it will be in the status that the gallium-nitride system compound semiconductor 2 grew only on sapphire by operation of this protective coat 11, and the wafer to which the selective growth of the gallium-nitride system compound semiconductor was carried out can be realized. Moreover, the protective coat 11 is formed in the chip configuration considered as a request at the line. (Since a chip configuration is usually a square, the protective coat 11 has been formed in a grid pattern.)

[0015] Moreover, the wafer shown in drawing 3 shows cutting, as a dashed line shows a protective coat 11 from the position which exfoliated, for example, can cut it half cutting or by carrying out full cutting by the dicer. Moreover, the wafer shown in drawing 4 can be broken and cut from the position shown with the dashed line of a scribe line by having ground the substrate and having made it thin. Since a scribe line can be put into direct silicon on sapphire by exfoliating a protective coat beforehand like drawing 4 , a wafer becomes easy to break. And there is no fear of separating, since the stress of a scriber does not start a gallium-nitride system compound semiconductor. When not exfoliating a protective coat 11, it is necessary to make the depth of a scribe line deep.

[0016] As shown in drawing 1 - drawing 4 , unless it makes line breadth of a protective coat 11 large and cutting plane lines, such as a scribe and dicing, are made to start the gallium-nitride system compound semiconductor layer 2, its gallium-nitride system compound semiconductor layer 2 is not hurt. Furthermore, if a protective coat 11 is exfoliated, a disconnection fraction serves as only silicon on sapphire 1, and stress does not start the gallium-nitride system compound semiconductor layer 2, but it can cut in the shape of a chip correctly.

[0017]

[Example] The mask of a predetermined configuration is formed in the silicon on sapphire 1 of 400 micrometers in [example 1] thickness, and size [of 2 inches] phi. After adhering SiO2 by vacuum evaporationo, sapphire is immersed in a solvent and a mask is removed from on the mask. Thereby, the pattern which consists of SiO2 protective coat 11 on 50 micrometers of line breadth, and 500 micrometer squares of a pitch on silicon on sapphire is completed. In this process, the plan of the silicon on sapphire involved the protective coat side is shown in drawing 5 .

[0018] The aforementioned silicon on sapphire is set to an MOCVD system, and on silicon on sapphire, it grows up by the thickness of 5 in all micrometers, and let an n type GaN layer and a p type GaN layer be gallium-nitride system compound semiconductor wafers. Although GaN grew on sapphire and transparence was presented when the wafer was picked out from equipment and the growth side was observed, nothing was growing on SiO2 protective coat.

[0019] After immersing the wafer to which the selective growth of the GaN was carried out as mentioned above in fluoric acid and exfoliating SiO2 protective coat, the silicon-on-sapphire side of a wafer is ground and thickness of a substrate is set to 100 micrometers.

[0020] Next, after sticking an adhesive tape on a silicon-on-sapphire side, setting to a scriber and fixing by the vacuum chuck, a scribe line is put in in the center of the line which exfoliated the protective coat in about 10 micrometer width of face and the depth of 5 micrometers. The partial expanded sectional view of a wafer which put in the scribe line is shown in drawing 6 . Thus, line breadth of SiO2 protective coat is beforehand made larger than the width of face of a scribe line, that is, the front face of a gallium-nitride system compound semiconductor and the side face are not damaged in the midst among a scribe to break by making line breadth of a protective coat larger than the disconnection width of face of a wafer.

[0021] The vacuum chuck was released after the scribe, the wafer was removed from the table, and much chips of 500 micrometer angle were obtained from the wafer of 2 inch phi by pressing down with a roller lightly from a silicon-on-sapphire side. When a crack, a chipping, etc. did not occur in the cut surface of a chip, GaN layer did not exfoliate, either but what has a poor appearance that is not was taken out, the yield was 95% or more.

[0022] In the process in which the [example 2] example 1 carries out a scribe, when stuck the adhesive tape on GaN layer side, and the scribe line was put in from the silicon-on-sapphire side, and also the chip of 500 micrometer angle was obtained similarly, similarly the yield was 95% or more. In addition, the scribe line by the side of silicon on sapphire also put the protective coat by the side of GaN layer into Chuo Line, the line which exfoliated.

[0023] In the process which forms the protective coat of the [example 3] example 1, the configuration of a mask is changed and pattern formation of the protective coat which consists of SiO2 is carried out in a grid pattern in 200 micrometers of line breadth, and 500 micrometer pitch.

[0024] Next, after carrying out the laminating of the GaN layer from on a protective coat similarly and creating a wafer, silicon on sapphire is ground and the thickness of a substrate is adjusted to 200 micrometers.

[0025] After sticking an adhesive tape on the silicon-on-sapphire side of the polished wafer and fixing to a dicer, the dicing of Chuo Line of a protective coat is carried out with the blade of 150 micrometer width of face, and full cutting of the wafer is carried out. The partial expanded sectional view of the wafer in the middle of this dicing process is shown in drawing 7 . This is also the same, line breadth of SiO2 protective coat is beforehand made larger than blade width of face, that is, the front face of a gallium-nitride system compound semiconductor and the side face are not damaged during a disconnection by making line breadth of a protective coat larger than the disconnection width of face of a wafer.

[0026] Much chips of 500 micrometer angle were obtained from the wafer after dicing. When a crack, a chipping, etc. similarly did not occur in the cut surface of a chip but what has a poor appearance that is not was taken out, the yield was 95% or more.

[0027] In the dicing process of the [example 4] example 3, when stuck the adhesive tape on GaN layer side, and full cutting was carried out from the silicon-on-sapphire side, and also the chip of 500 micrometer angle was obtained similarly, similarly the yield was 95% or more.

[0028]

[Effect of the invention] As explained above, according to the technique of this invention, the gallium-nitride system compound semiconductor wafer which does not have cleavage nature can also be correctly cut with a sufficient yield using various disconnection equipments, and its productivity improves.

[Translation done.]